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Chipmetrics is a forerunner in productizing test structures, test chips and monitoring wafer concepts for advanced materials and microelectronics manufacturing.

Since	2019
Expertise	Conformal coatings, High aspect ratio structures, 3D metrology.
Country	Finland
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IN-PROCESS CONFORMAL TESTING WITH PILLARHALL® LHAR4

by Mikko Utriainen

The downscaling of future semiconductor devices with increasing 3D character results to increasing demand for highly conformal thin films. Conformal deposition provides also new opportunities in microelectromechanical systems (MEMS), photonics, and other material science applications. Conformality is a core value proposition of Atomic Layer Deposition (ALD), and also obtained in Chemical Vapor Deposition (CVD) processes in certain conditions. The conformality is challenging to measure and quantify, and standardized measurement methods do not exist. Traditional vertical high aspect ratio test structures rely typically on time-consuming and expensive cross-sectional SEM/TEM analyses while unique and innovative PillarHall® lateral high aspect ratio (LHAR) test structure enables easy, cost-efficient and accurate measurements of thin film conformality. It is also compatible to efficient and fast optical measurement methods. This white paper describes the standard procedure of LHAR measurement method in 3D thin film process monitoring.

PILLARHALL Lateral High Aspect Ratio (LHAR) Test Chip provides fast and accurate thin film conformality data source. The PillarHall LHAR chip is used in ALD/CVD deposition as a measurement tool and a referencing platform. The PillarHall LHAR4 test chip is productized and made commercially available by Chipmetrics Ltd. Company delivers the test chips to customers all over the world.

The users are typically ALD and conformal 3D thin film process and equipment developers as well the industrial users of ALD processes. Chipmetrics core expertise is in Atomic Layer Deposition (ALD). Company headquarters are in Finland – in the country of the origin of ALD.

1. PillarHall® LHAR4-Lateral High Aspect Ratio Silicon Test Chip

PillarHall test chip is all-silicon chip with multiple lateral high aspect ratio structures helping the determination of the quality of the deposited thin film.

1.1 Description of the chip

PillarHall LHAR test structures consists of 500 nm lateral gap height under a silicon membrane supported by silicon pillars. One PillarHall test chip consist over 20 lateral high aspect ratio test structures where aspect ratio varies from 2:1 to 10000:1. The name PillarHall comes from the microscopic silicon pillars that stabilize the thin silicon membrane roof. This lateral 3D approach is the core invention of the PillarHall® technology. The test structure enables fast analysis and accuracy for the measurement. Conformality is measured and quantified from the film penetration depth profile from the extreme high aspect ratio structures. The film penetration depth profile is a unique and informative experimental data. It is obtained by measuring film thickness as a function of depth distance at the LHAR lateral high aspect ratio trench. The penetration depth

profile enables to quantify film conformality and eg. to extract various reaction kinetics factors.



Fig. 1 – Layout of the PillarHall LHAR4 test chip.

Up to now, typical aspect ratios greater than 50 can be found in advanced semiconductor 3D devices and aspect ratios over 1000 in most demanding applications. It expected to see in a near future even higher values due to further development of deep etching and conformal deposition processes and the rise of stacked layered structures (3D NAND) and heterogenous integration.

1.2 Experimental procedure

Typically, the test chip is placed at the center of a carrier wafer for monitoring the deposition quality. It may happen that during the deposition, the chip moves, to avoid such an issue, the carrier wafer may contain etched pocket holder for the 15 × 15 mm² LHAR4 chip.

It is often seen that during a deposition process, the conformality varies from a wafer area to another. This depends on the system and on the process itself. Therefore, the exact positioning of the chip on the carrier wafer has a crucial importance and the obtention of reliable and reproducible results rely on a positioning at similar place in the deposition chamber through the runs.

A schematic view of the LHAR structure is given in Fig. 2. One can see the silicon membrane and a conformal layer. The conformality is analysed by lateral scan measurement to determine the details of the penetration depth area (x_p) of the film under the membrane.

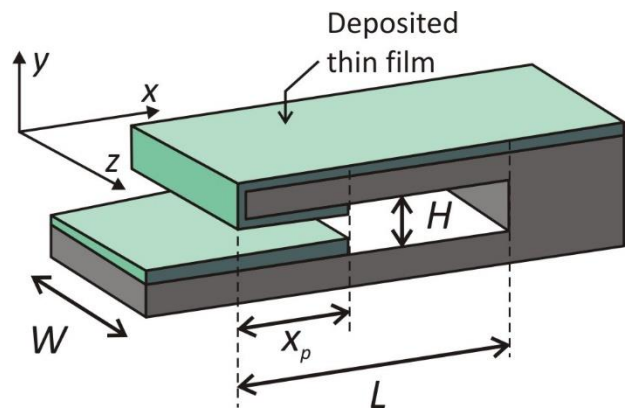


Fig. 2 – Test structure and the principle of LHAR measurement method. H stands for the gap height ($H=500$ nm for LHAR4). L is the length of the cavity, W is the width of the trench opening, x_p is the film penetration depth allowing the determination of the conformality, such as penetration depth, of the thin film.

Using several test chips positioned at different locations on the carrier wafer, it is possible to monitor the conformality of the deposition at the wafer level. Typical use in that case is 5 to 9 chips on a carrier wafer for one deposition run.

In order to perform an accurate measurement of the conformality, the top membrane has to be removed, see Fig. 3, simply using an adhesive tape.



Fig. 3 – Illustration of the removal of the top membrane with an adhesive tape.

2. Measurement methodology

2.1 Techniques

Once the deposition is done, the test chip can be removed from the carrier wafer and measured with an optical microscope for instance. Although the use of the PillarHall chip is relatively straightforward, its analysis requires some practice.

A typical use is optical metrology measurements. Most common tools are optical microscope, reflectometer line-scanner, and ellipsometer line-scanner. A summary of the instrumentation typically used for the analysis of the test chips is given in Table 1 below.

Table 1 – Typical tools, with corresponding specifications, used for the analysis of the chip.

Instrument	Specifications
Optical digital microscope	20-50× magnification, efficient illumination and optics, filters are useful.
Reflectometer line-scanner	Spot size preferably smaller than 10 μm .
Ellipsometer line-scanner	Spot size smaller than 50 μm .

In addition, several other metrology tools are compatible with the chip for its analysis. However, they require some specificity:

- Versatile lateral scanning area 50-1000 μm (x , or xy),
- Height resolution < 1 nm (z),
- Lateral resolution < 5 microns (xy).

In the optical microscope measurement, digital images are captured for further image analysis, which can be performed by the user itself or by using Chipmetrics' service. Fig. 4 is an example of image that can be acquired from the microscope.

In the spectrometer line scanners, when applicable to the thin film sample material, the instrument outcome is directly the film thickness. The scanner stage must be carefully placed so that the measurement starts at a point where the membrane edge position can be identified.

Generally, microscope and reflectometer sensitivities are limited by the film thickness (requires preferably > 20 nm in thickness) while ellipsometer is compatible to lower thickness (< 10 nm). However, ellipsometer has typically lower lateral resolution than optical microscope or reflectometer.



Fig. 4 – A typical microscope image of LHAR test structure showing film penetration (dark area) and distance markers on the chip.

2.2 Data for processing monitoring

The standard measurement procedure aims at to obtain numerical values for the film penetration depth profile. The profile is the film thickness as a function of the film penetration distance. Fig. 5 illustrates a typical penetration depth profile.

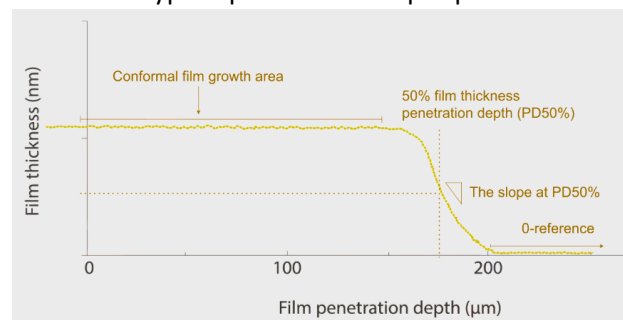


Fig. 5 – Typical penetration depth profile and characteristic values for the conformity [4].

The film penetration depth profile allows to determine characteristic values for conformity. The penetration depth is a distance corresponding to a particular film thickness given as a percentage of the initial value of the deposited film. The recent scientific literature [1-4] has proposed to use the penetration depth 50%, i.e., PD50% corresponds to a penetration distance point where the film thickness has 50% of its initial value. Additionally, the slope at the PD50% position can be useful when modelling the reaction kinetics [2], especially in ALD processed.

The measurement provides PD50% unit in meters. Since the penetration depth depends strongly on the aspect ratio, the PD50% value is typically normalized to a dimensionless distance, PD50%(AR). It

is defined by Eq. (1), in a similar way than the aspect ratio:

$$PD50\% (AR) = \frac{PD50\%(L)}{H}, \quad (1)$$

where PD50%(L) is the measured penetration depth and H is the gap height (H = 500 nm) in the case of the PillarHall LHAR4 test chips.

Finally, using several test chips, it is possible to perform a mapping of the conformality at the wafer-scale. Fig. 6 is an example showing the different values of penetration of the film under the membrane during deposition of TiO₂ in an ALD reactor.

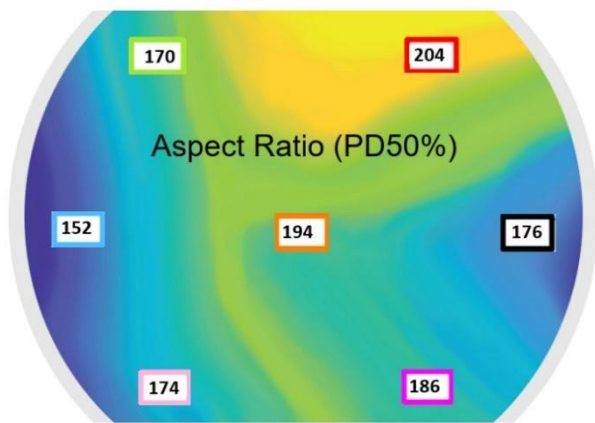


Fig. 6 – Example of mapping of conformality over a full wafer. More details can be found in reference [4] and other technical notes available on the website of the company or by contacting directly Chipmetrics.

References

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